

Amendments to the Claims:

Please cancel claims 1-26 without prejudice or disclaimer to the pursuit of the subject matter thereof in a divisional application.

No claims have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-26 (Canceled)

27. (Original) A semiconductor wafer having an active surface and a backside surface and including a plurality of semiconductor dice formed thereon, wherein:
the active surface includes integrated circuitry thereon;
the backside surface is in a back-ground state;
a solid material extends over and is bonded to the backside surface; and
an interface between the backside surface and the solid material has a mean surface roughness factor R_a of between about 5% and about 40% of a mean thickness of the semiconductor wafer.

28. (Original) The semiconductor wafer of claim 27, wherein semiconductor material of the semiconductor wafer comprises one of silicon, gallium arsenide, germanium and indium phosphide.

29. (Original) The semiconductor wafer of claim 27, wherein the interface has a mean surface roughness factor R_a between about 2 μm and about 15 μm .

30. (Original) The semiconductor wafer of claim 27, wherein the solid material comprises a polymer.

31. (Original) The semiconductor wafer of claim 27, wherein the solid material includes at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and ParylenesTM.
32. (Original) The semiconductor wafer of claim 27, wherein the solid material comprises one of a thermoset cross-linkable polymer, a UV cross-linkable polymer and a two-part epoxy.
33. (Original) The semiconductor wafer of claim 27, wherein the solid material comprises a ParyleneTM polymer.
34. (Original) The semiconductor wafer of claim 27, wherein the solid material has a mean thickness of about 100 μm or less over a highest topographic feature on the backside surface.
35. (Original) The semiconductor wafer of claim 27, wherein the solid material has a mean thickness of about 10 μm or less over a highest topographic feature on the backside surface.
36. (Original) The semiconductor wafer of claim 27, wherein the solid material has a generally planar exposed surface.
37. (Original) The semiconductor wafer of claim 27, wherein the solid material comprises an ionic barrier.
38. (Original) The semiconductor wafer of claim 27, wherein the semiconductor wafer has a thickness of about 4 mils or less.

39. (Original) The semiconductor wafer of claim 27, wherein the semiconductor wafer has a thickness of about 2 mils or less.

40. (Original) The semiconductor wafer of claim 27, wherein the semiconductor wafer has a nominal diameter of at least about 200 mm (about 8 inches).

41. (Original) The semiconductor wafer of claim 27, wherein the semiconductor wafer has a nominal diameter of at least about 300 mm (about 12 inches).

42. (Original) The semiconductor wafer of claim 27, wherein material of the semiconductor wafer is in a state of compression.

43. (Original) A semiconductor package, comprising:
a die of semiconductor material having an active surface and a backside surface;
integrated circuitry on the active surface;
wherein the backside surface is in a roughly back-ground state and includes a solid material
extending thereover and bonded thereto;
a protective material encapsulating at least a portion of the die and the solid material extending
over the backside surface; and
a plurality of conductive terminals exposed through the protective material on a surface of the
package;
wherein an interface between the backside surface and the solid material has a mean surface
roughness factor R_a of between about 5% and about 40% of the mean thickness of the die.

44. (Original) The package of claim 43, wherein the interface has a mean surface roughness factor R_a of between about 2 μm and about 15 μm .

45. (Original) The package of claim 43, wherein the solid material comprises a polymer.

46. (Original) The package of claim 43, wherein the solid material includes at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and Parylenes™.

47. (Original) The package of claim 43, wherein the solid material comprises one of a thermoset cross-linkable polymer, a UV cross-linkable polymer and a two-part epoxy.

48. (Original) The package of claim 43, wherein the solid material comprises a Parylene™ polymer.

49. (Original) The package of claim 43, wherein the semiconductor material of the die is in a state of compression.

50. (Original) A semiconductor wafer having a thickness of about 4 mils or less and which maintains an unwarped state in an absence of external force applied thereto.

51. (Original) The semiconductor wafer of claim 50, wherein the thickness is about 2 mils or less.

52. (Original) The semiconductor wafer of claim 50, wherein material of the semiconductor wafer is in a state of compression.